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### 54 Multiplying circuit.

57 Disclosed is a multiplying circuit in which a pair of common-base transistors (13, 14) each having a small emitter area are inserted between the common emitter terminals of first and second differential amplifiers (1,2 ; 3,4), which amplify a signal input to an input terminal pair and are connected in such a way as to cancel out their outputs which correspond to the input signal, and the output terminal pairs of multiple third differential amplifiers (5,6 ; 7,8), which amplify a signal input to another input terminal pair and have a predetermined DC offset characteristic.

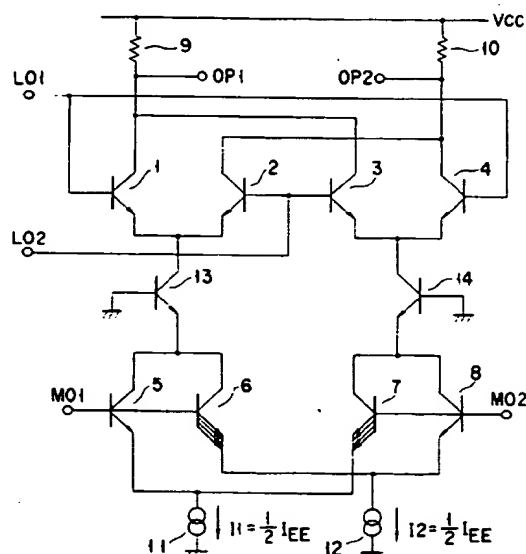


FIG. 1

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The present invention relates to a multiplying circuit which comprises differential amplifiers and are adapted for use in a frequency converter, a synchronous detector, a quadrature modulator, a demodulator, a variable gain amplifier, etc.

Conventional multiplying circuits have two pairs of input terminals respectively supplied with two input signals to be multiplied. The input signal input to one input terminal pair is amplified by a first differential amplifier and a second differential amplifier. The output terminal pairs of the first and second differential amplifiers are connected together in such a way that the outputs of those differential amplifiers with respect to the first input signal will cancel out each other. A second input signal input to the other input terminal pair is amplified by a third differential amplifier to be converted into a change in the collector current of transistors constituting this differential amplifier.

Since the first and second differential amplifiers have their common emitter terminal connected to the collector of the collectors of the transistors of the third differential amplifier, the gains of the first and second differential amplifiers are proportional to the collector current of the transistors of the third differential amplifier. Therefore, a voltage proportional to the product of voltages of the first and second input signals or a multiplied output is yielded between the common output terminal of the first and second differential amplifiers.

Such a multiplying circuit will have a deformed output signal waveform because of the non-linearity of the differential amplifiers as the voltage amplitudes of the input signals get large. As a solution to this shortcoming has been proposed an art of constituting the third differential amplifier with a combination of two differential amplifiers and providing the proper DC offset to these differential amplifiers to widen the linearity range as disclosed in U.S. Patent No. 4,965,528. The DC offset of the differential amplifier is determined by the emitter area of a pair of emitter coupled transistors constituting this differential amplifier.

Another multiplying circuit has also been proposed which combines three or more differential amplifiers to constitute the third differential amplifier in order to ensure a wider linearity range. How to give a DC offset to the differential amplifiers and weight a current to each differential amplifier in this case is disclosed in Electronic Circuit Study Report No. ECT-90-20 of Electric Committee and "Realization of a 1-V Active Filter Using a Linearization Technique Employing Plurality of Emitter-Coupled Pair", IEEE JOURNAL OF SOLID-STATE CIRCUITS, pages 937-944, VOL. 26, NO. 7, JULY 1991.

In this method, however, as the number of third differential amplifiers increases, their transistors should have a larger emitter area, increasing the parasitic capacitance of the transistors so that the use of

the multiplying circuit at a high frequency becomes difficult. For instance, given that the emitter area ratio of one pair of emitter coupled transistors constituting the third differential amplifier is 1 : 4, the sum of the parasitic capacitances present between the collectors of the emitter coupled transistors and the ground becomes about five times greater than that of the previously described conventional multiplying circuit. As the frequency of the first input signal increases, therefore, the CMRR (Common Mode Rejection Ratio) of the first and second differential amplifiers falls. In addition, the frequency rise will increase signals that leak to the second input terminal pair from the first input terminal pair through the collector-base parasitic capacitance.

The drop of the CMRR causes a local oscillator signal to the transmission output side to increase, in the case the multiplying circuit is used as a frequency converter or a modulator in a transmitter, for example, with a local oscillator signal and a transmission signal respectively given as the first and second input signals to the frequency converter or the modulator. With the multiplying circuit used as a frequency converter in a receiver, for example, when the number of signals leaking to the second input terminal pair from the first input terminal pair increases, the local oscillator signal input to the first input terminal pair will increase the undesirable radiation from an antenna via the second input terminal pair, a high frequency amplifier and the like.

The conventional ways of broadening the linearity range can apply only to the third differential amplifier side to which the second input signal is to be input, and cannot widen the linearity ranges of the first and second differential amplifiers. This undesirably causes the first input signal component to be easily deformed.

If the frequencies of the first and second input signals are relatively apart from that of the desired output signal as in a frequency converter or a demodulator, a multiplying circuit comprising a half circuit components of the first described conventional multiplying circuit is often used. That is, this multiplying circuit comprises a first differential amplifier connected to a first input terminal pair, and a common-emitter transistor connected to the common emitter of the transistors of the first differential amplifier. The first and second input terminal pairs of this multiplying circuit are supplied with two input signals to be multiplied, the second input terminal pair connected to the base of the common-emitter transistor. The first input signal input to the first input terminal pair is amplified by the differential amplifier, while the second input signal input to the second input terminal pair is amplified by the common-emitter transistor. A multiplied output of the first and second input signals is acquired from an output terminal provided in a load circuit of the differential amplifier.

This multiplying circuit if used as a frequency converter or a demodulator in a receiver has a disadvantage of having an insufficient noise factor. The noise generated in the multiplying circuit is mainly thermal noise from the parasitic resistor of the base of the common-emitter transistor. The thermal noise can be reduced by setting the emitter area of the common-emitter transistor larger or increasing the base area.

Increasing the emitter area of the common-emitter transistor however would result in a decrease in the CMRR of the differential amplifier and an increasing in the signals leaking from the first input terminal pair to the second input terminal pair, as happened in the first described conventional multiplying circuit which comprises three differential amplifiers to improve the linearity. In a direct conversion-type receiver, particularly, the reception frequency is nearly equal to the local oscillator frequency, so that when a local oscillator signal is input to the first input terminal pair and a reception signal to the second input terminal pair, the local oscillator signal will leak through the second input terminal pair. This gives rise to a significant problem.

In short, the first described multiplying circuit designed to improve the linearity range has the following two disadvantages:

- 1) The CMRR of the differential amplifier decreases in a high frequency range (radio frequency band) due to an increase in the parasitic capacitance of transistors in use and the degree of one input signal leaking from one input terminal pair to the other input terminal pair increases.
- 2) Widening of the linearity range is accomplished only to one of two input signals, resulting in insufficient suppression of the deformation of the other input signal.

Further, the use of a common-emitter transistor having a large emitter area to improve the noise factor in the second described conventional multiplying circuit would also result in undesirable reduction of the CMRR of the differential amplifier in a high frequency range and increase in the degree of one input signal leaking from one input terminal pair to the other input terminal pair.

It is therefore an object of the present invention to provide a multiplying circuit which can prevent the reduction of the CMRR on the high frequency side due to the parasitic capacitance of a transistor and can suppress the degree of a signal leaking from one input terminal pair to another input terminal pair.

It is another object of this invention to provide a multiplying circuit capable of widening the linearity range of a differential amplifier to both input terminals thereby achieve lower signal deformation.

According to one aspect of the present invention, there is provided a multiplying circuit which basically has a common-base transistor inserted between an amplifier section for a first input signal and an amplifier

section for a second input signal.

That is, a multiplying circuit designed for higher linearity has common-base transistors inserted respectively between a common emitter terminal of first and second differential amplifiers for amplifying a first input signal and output terminal pairs of multiple third differential amplifiers for amplifying a second input signal. More specifically, the multiplying circuit comprises first and second differential amplifiers, which receive a first input signal and each have an output terminal pair and a common emitter terminal; an output circuit for connecting the output terminal pairs of the first and second differential amplifiers in such a way as to cancel out outputs of the first and second differential amplifiers, which correspond to the first input signal, each other, and providing a difference between the outputs of the first and second differential amplifiers as an output signal; first and second common-base transistors having bases grounded in AC mode and collectors connected to the common emitter terminals of the first and second differential amplifiers; and multiple third differential amplifiers each having an output terminal pair connected commonly to emitters of the first and second common-base transistors and each given with a predetermined DC offset.

The multiplying circuit may comprise a plurality of first and second differential amplifiers, in which case a plurality of first and second common-base transistors are provided. This design can provide a DC offset to the first and second differential amplifiers.

According to another aspect of the present invention, there is provided a multiplying circuit for amplifying a second input signal by means of a common-emitter transistor has such a common-emitter transistor inserted between a common emitter terminal of a differential amplifier and the collector of the common-emitter transistor. More specifically, the multiplying circuit comprises a differential amplifier, which receives a first input signal and has an output terminal pair and a common emitter terminal; a load circuit connected to at least one output terminal of the output terminal pair of the differential amplifier; a common-emitter transistor having a base supplied with a second input signal; and a common-base transistor having a base grounded in an AC manner, a collector connected to the common emitter terminal of the differential amplifier; and an emitter connected to a collector of the common-emitter transistor and having a smaller emitter area than the common-emitter transistor.

When the first and second common-base transistors are inserted between the common emitter terminal of the first and second differential amplifiers and output terminal pairs of multiple third differential amplifiers, the emitter areas of these common-base transistors can be made smaller than the largest emitter area of transistors used in the third differential

amplifiers. An impedance as viewed toward the output terminal pair side of the third differential amplifier from the common emitter terminal of the first and second differential amplifiers therefore becomes larger than the one yielded in a multiplying circuit without those common-base transistors.

Even if the emitter area of some transistor in the third differential amplifier is increased to give a DC offset to that transistor, therefore, it is possible to prevent the CMRR of the first and second differential amplifiers from falling due to the large parasitic capacitance of the transistor and reduce the degree of a signal leaking from the first input terminal pair to the second input terminal pair.

Further, provision of multiple first and second common-base transistors and provision of multiple first and second differential amplifiers to impart a DC offset to the first and second differential amplifiers can widen not only the linearity to the first input signal but also the linearity to the second input signal, accomplishing lower signal deformation in the whole multiplying circuit.

With a common-base transistor inserted between the common emitter terminal of the differential amplifier for amplifying the first input signal and the collector of the common-emitter transistor for amplifying the second input signal, even when a transistor with a large area is used as the common-emitter transistor in order to reduce the parasitic resistance of the base, the CMRR of the differential amplifier is prevented from falling the degree of a signal leaking from the first input terminal pair to the second input terminal pair is suppressed because of the above-described principle. Although the parasitic resistance of the base of the common-base transistor is large, thermal noise originating from this parasitic resistance hardly appears on the output due to the negative feedback effect caused by the output impedance of the common-emitter transistor. The noise factor of the multiplying circuit can be improved while increasing the area of the common-emitter transistor.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram of a multiplying circuit according to a first embodiment of the present invention;

Fig. 2 is a diagram illustrating the frequency response of a carrier leak at the output terminal of the multiplying circuit shown in Fig. 1;

Fig. 3 is a diagram illustrating the frequency response of a carrier leak at the input terminal of the multiplying circuit shown in Fig. 1;

Fig. 4 is a circuit diagram of a multiplying circuit according to a second embodiment of the present invention;

Fig. 5 is a circuit diagram of a multiplying circuit according to a third embodiment of the present

invention;

Fig. 6 is a circuit diagram of a multiplying circuit according to a fourth embodiment of the present invention;

Fig. 7 is a circuit diagram of a multiplying circuit according to a fifth embodiment of the present invention;

Fig. 8 is a circuit diagram showing a modification of the first embodiment;

Fig. 9 is a circuit diagram showing a modification of the second embodiment;

Fig. 10 is a circuit diagram showing a modification of the third embodiment;

Fig. 11 is a circuit diagram showing a modification of the fourth embodiment;

Fig. 12 is a circuit diagram showing a modification of the fifth embodiment;

Fig. 13 is a circuit diagram of a multiplying circuit according to a sixth embodiment of the present invention;

Fig. 14 is a circuit diagram of a multiplying circuit according to a seventh embodiment of the present invention;

Fig. 15 is a circuit diagram of a multiplying circuit according to an eighth embodiment of the present invention; and

Fig. 16 is a circuit diagram of a multiplying circuit according to a ninth embodiment of the present invention.

In Fig. 1, two input signals to be multiplied are input to two pairs of input terminals, LO1 and LO2, and MO1 and MO2. The first input signal input to the input terminal pair LO1 and LO2 is amplified by a first differential amplifier comprising transistors 1 and 2, and a second differential amplifier comprising transistors 3 and 4. A pair of output terminals (collectors of the transistors 1 and 2) of the first differential amplifier are connected to a pair of output terminals (collectors of the transistors 3 and 4) of the second differential amplifier in such a way that the outputs of both differential amplifiers to the first input signal cancel out each other. The first and second differential amplifiers have their output terminal pairs connected to one ends of load resistors 9 and 10 as well as a pair of output terminals OP1 and OP2 of a multiplying circuit.

In the first differential amplifier, the transistor 1 with a base connected to the input terminal LO1 has the collector connected to the load resistor 9 and the output terminal OP1, and the transistor 2 with a base connected to the input terminal LO2 has the collector connected to the load resistor 10 and the output terminal OP2. In the second differential amplifier, however, the transistor 3 with a base connected to the input terminal LO1 has the collector connected to the load resistor 10 and the output terminal OP2, and the transistor 4 with a base connected to the input terminal LO2 has the collector connected to the load resistor 9 and the output terminal OP1. The other ends of

the resistors 9 and 10 are connected to a voltage supply Vcc.

First and second common-base transistors 13 and 14 whose bases are grounded in an AC manner have their collectors respectively connected to a common emitter terminal of the transistors 1 and 2 of the first differential amplifier and that of the transistors 3 and 4 of the second differential amplifier.

The second input signal input to the input terminal pair MO1 and MO2 is amplified by two third differential amplifiers respectively comprising transistors 5 and 7, and transistors 6 and 8. The common emitter terminals of the third differential amplifiers are connected to constant current sources 11 and 12.

Output terminal pairs of the third differential amplifiers are connected in common to the emitters of the common-base transistors 13 and 14. That is, the collectors of the transistors 5 and 6 are commonly connected to the emitter of the first common-base transistor 13, and the collectors of the transistors 7 and 8 are commonly connected to the emitter of the second common-base transistor 14.

The two transistors constituting each third differential amplifier have a predetermined emitter area ratio. In this embodiment, the emitter area ratio of the transistor 6 to the transistor 7 is about four times greater than that of the transistor 5 to the transistor 8. Such setting of the emitter area ratios will give a DC offset to the two third differential amplifiers with respect to the second input signal from the input terminal pair MO1 and MO2. Synthesizing the outputs of the differential amplifiers therefore widens the linearity range of the third differential amplifiers. The principle of expanding the linearity range by the DC offset is well known, and its detailed explanation will not therefore be given.

The first and second differential amplifiers which amplify the first input signal have their common-emitter terminals linked to the pair of the output terminals of the third differential amplifiers through the common-base transistors 13 and 14 respectively. The gains of the first and second differential amplifiers are therefore proportional to the collector current in the third differential amplifiers which amplify the second input signal. Between the output terminals OP1 and OP2 is obtained an output signal whose voltage amplitude is proportional to the product of the first and second input signals. The circuit shown in Fig. 1 therefore serves as a multiplying circuit.

The common-base transistors 13 and 14 have an emitter area smaller than the maximum emitter area of the transistors (emitter area of the transistors 6 and 7) in the third differential amplifiers, and also has a smaller parasitic capacitance. If the emitter area of the common-base transistors 13 and 14 is the same as that of the transistors 5 and 8 in the third differential amplifiers, and the emitter area of the transistors 6 and 7 is about five times that of the transistors 5 and

8, the parasitic capacitance of the transistors 13 and 14 becomes approximately 1/5. In a high frequency range, therefore, an impedance as viewed from the common emitter terminals of the first and second differential amplifiers toward the third differential amplifiers is high, compared with the conventional case where the common-base transistors 13 and 14 are not provided and the linearity range of the third differential amplifiers is widened by connecting the collectors thereof directly to the common emitter terminals of the first and second differential amplifiers. The CMRR (Common Mode-Rejection Ratio) of the first and second differential amplifiers rises at a high frequency accordingly.

Fig. 2 illustrates effects of the CMRR confirmed by computer simulation. Generally, a multiplying circuit of this type has one of the input terminals of a differential amplifier grounded in AC mode. In the multiplying circuit in Fig. 1, therefore, a sine wave is input to the input terminal LO1, thereby yielding the frequency response of a carrier leak at the output terminal OP1 when the input terminal LO2 is grounded in an AC manner. Fig. 2 shows the frequency response. In Fig. 2, a curve A shows the carrier leak of the multiplying circuit in Fig. 1, a curve B presents the carrier leak of the multiplying circuit excluding the common-base transistors 13 and 14 in Fig. 1, and a curve C shows the carrier leak of the conventional basic multiplying circuit.

When a signal only consisting of difference components is input between the input terminal pair LO1 and LO2, the carrier leak is -100 dB or below. The curves in Fig. 2 therefore show the carrier leaks for a common mode. As shown by the curve A, the multiplying circuit in Fig. 1 has lower carrier leak in the all frequency ranges than the multiplying circuit without the common-base transistors 13 and 14. Particularly in a low frequency range, the carrier leak of the multiplying circuit in Fig. 1 is reduced by about 30 dB, and is about 8 dB less than that of the conventional multiplying circuit. According to the present invention, the improvement on the CMRR is apparent.

In a case where the multiplying circuit is used as the frequency converter or modulator of a transmitter, and a local oscillator signal and a transmission signal are input respectively as the first and second input signals, a carrier leak to a transmission output side can be decreased.

Further, since the changes of collector voltages in the common-base transistors 13 and 14 are transmitted less to their emitters, the transistors 5 and 6 have a smaller change in their collector voltages. Accordingly, the carrier leak from the input terminal LO1 to the input terminal MO1 is reduced.

As a result, if the multiplying circuit, when used as the frequency converter of a receiver, receives a local oscillator signal from a local oscillator between the input terminals LO1 and LO2, and a reception signal

between the input terminals MO1 and MO2, it is possible to decrease the amount of the local oscillator signal that leaks from input terminals MO1 and MO2 and leaves as undesirable radiation from an antenna via a high frequency amplifier, etc.

Fig. 3 illustrates the results of the reduction in the carrier leak confirmed by computer simulation, and shows the frequency response of the carrier leak to the input terminal MO1 with the same input as in the case of Fig. 2 applied between the input terminal pair LO1 and LO2. In Fig. 3, a curve D shows the carrier leak of the multiplying circuit in Fig. 1; a curve E the carrier leak of the multiplying circuit excluding the common-base transistors 13 and 14 in Fig. 1; a curve F the carrier leak of the conventional basic multiplying circuit. The curve D shows the lower carrier leak in all frequency ranges than the curves E and F. Particularly, in a low frequency range, the carrier leak of the multiplying circuit in Fig. 1 is 40 dB less than that of the basic multiplying circuit. The decrease in the carrier leak according to the present invention is apparent.

Another embodiment of the present invention will now be described. Fig. 4 illustrates a multiplying circuit according to the second embodiment, which ensures a larger linearity range by the combination of four third differential amplifiers. The four third differential amplifiers comprise pairs of differential transistors 21 and 25, 22 and 26, 23 and 27, and 24 and 28, and constant current sources 31 to 34, respectively. The constant current sources 31-34 are connected to the corresponding common emitter terminals of the transistor pairs. If the emitter area ratio of the transistors 21 and 28, to the 22 and 27, and to the transistors 23-26 is determined to be 13 : 2 : 1, for example, a DC offset is given to the individual differential amplifiers. In other words, four pairs of transistors 21, 25; 22, 26; 23, 27; and 24, 28 have emitter area ratios of 13 : 1; 2 : 1; 1 : 2; and 1 : 13, respectively. The currents of the constant current sources 31 to 34 are weighted by determining the current ratio of the constant current sources 31 to 34 as shown in Fig. 4.

The number of the differential amplifiers may be three or five or greater, and has only to be selected in accordance with the required linearity range. As the number of the differential amplifiers is increased, transistors with a larger emitter area are needed as apparent from the example shown in Fig. 4, increasing the parasitic capacitance accordingly, so that the improvement on the frequency response by the provision of the common-base transistors 13 and 14 becomes more prominent.

Fig. 5 illustrates a multiplying circuit according to the third embodiment in which there are two first differential amplifiers and two second differential amplifiers, with the same number of first and second common-base transistors. More specifically, the first differential amplifier comprises a differential transistor

pair 41 and 43 and a differential transistor pair 42 and 44, and the second differential amplifier comprises a differential transistor pair 45 and 47 and a differential transistor pair 46 and 48. By determining the emitter area ratio of the transistors 41, 44, 45 and 48 to the transistors 42, 43, 46 and 47 to 4 : 1, for example, a DC offset is given to the first and second differential amplifiers. In other words, two pairs of transistors 41, 43; and 42, 44 have emitter area ratios of 4 : 1; and 1 : 4, respectively. Similarly, two pairs of transistors 45, 47; and 46, 48 have emitter area ratios of 4 : 1; and 1 : 4, respectively.

Two common emitter terminals of the first differential amplifier are connected to the collectors of the first common-base transistors 58 and 59, while two common emitter terminals of the second differential amplifier are connected to the collectors of the second common-base transistors 60 and 61. Three third differential amplifiers are constituted by transistors 49 to 54, and constant current sources 55 to 57, respectively. One terminal of the common output terminal pair of those third differential amplifiers (the common collector terminal of the transistors 49 to 51) is connected in common to the emitters of the first common-base transistors 58 and 59. The other terminal of this common output terminal pair (the common collector terminal of the transistors 52 to 54) is connected in common to the emitters of the second common-base transistors 60 and 61.

According to this embodiment, a DC offset can be given to the first and second differential amplifiers by the provision of multiple first and second common-base transistors and provision of multiple first and second differential amplifiers, so that the linearity also to the first input signal to be applied to the input terminal pair LO1 and LO2 can be widened. The multiplying circuit according to this embodiment is therefore suitable for a use in which both input signals are information signals and linearity to both inputs is required over a wide frequency range.

Fig. 6 shows a multiplying circuit according to the fourth embodiment which are provided with three first and second differential amplifiers constituted by transistors 71 to 82 and three third and fourth common-base transistors 91-93 and 94-96. The third differential amplifiers comprise transistors 83 to 88 and constant current sources 97 to 99.

In this embodiment, the emitter area ratio of the transistors 71, 76, 77 and 82 to the transistors 72-75 and 78-81 in the first and second differential amplifiers is determined to be 8 : 1, and the emitter area ratio of the common-base transistors 91, 93, 94 and 96 to the transistors 92 and 95 is determined to be 3 : 2, for example, a DC offset is given to the first and second differential amplifiers, and a collector current proportional to the emitter area will flow through the common-base transistors. It is therefore possible to weight the distribution ratio of the emitter currents to

the first and second differential amplifiers.

In the third differential amplifiers, as the emitter area ratio of the transistors 83 and 88 to the transistors 84-87 is determined to be 8:1, for example, and the current ratio of the constant current sources 97 to 99 is set as given in Fig. 6, a DC offset is given to the individual differential amplifiers and the current weighting is performed.

The use of the weighting system in this embodiment can permit the whole multiplying circuit to be constituted by either npn type transistors or pnp type transistors. In general, npn transistors have a better frequency response than pnp transistors in an integrated circuit. The feature of this embodiment to allow a multiplying circuit to be constituted by npn transistors alone is advantageous to improve the frequency response of the multiplying circuit.

Fig. 7 illustrates a multiplying circuit according to the fifth embodiment in which common-base transistors 105 to 110 having a small emitter area are inserted between the common emitter terminals of first and second differential amplifiers in Fig. 6 and weighting common-base transistors 91 to 96. This embodiment therefore has an effect of suppressing the reduction of the CMRR caused by transistors with a large emitter area and large parasitic capacitance, contained in the weighting common-base transistors 91-96, in addition to the advantage of the fourth embodiment in Fig. 6. In this embodiment the third differential amplifiers are constituted by transistors 101 to 104 and constant current sources 111 and 112, the emitter area ratio of the transistors 101 and 104 to the transistors 102 and 103 is determined to be 4:1, for example, and the current ratio of the constant current source 111 to the constant current source 112 is set as given in Fig. 7.

Figs. 8 through 12 respectively illustrate multiplying circuits according to modifications of the first to fifth embodiments in which an input terminal pair LO1 and LO2, an input terminal pair LO3 and LO4, and an input terminal pair MO1 and MO2 are applied with input signals and the proper DC bias potentials, while base terminals VB1, VB2, VB3 and VB4 of common-base transistors are applied with the proper DC bias potentials and are grounded in an AC manner. It is obvious that the above designs can accomplish the same operations as the previously described embodiments.

Although the first input signal and second input signal are both input to differential amplifiers in the above-described embodiments, the first input signal may be input to the differential amplifiers while inputting the second input signal to a common-emitter amplifier. The following will describe such an embodiment.

Fig. 13 shows a multiplying circuit according to the sixth embodiment in which the first input signal is input to an input terminal pair LO1 and LO2 and the

second input signal to another input terminal Rf. The first input signal input to the input terminal pair LO1 and LO2 is amplified by a differential amplifier comprising transistors 201 and 202. This differential amplifier has its output terminal pair (the collectors of the transistors 201 and 202) connected via a load circuit 203 to a voltage supply Vcc. In this example, the load circuit 203 is constituted by a current-mirror circuit comprising transistors 204 and 205, with the collector of the transistor 205 connected to an output terminal OP.

The second input signal input to the input terminal Rf is amplified by a common-emitter transistor 207, which has its base connected to the input terminal Rf and its emitter grounded.

A common emitter terminal of the transistors 201 and 202 in the differential amplifier is connected to the collector of the common-base transistor 206 whose emitter is connected to the collector of the common-emitter transistor 207. The common-base transistor 206 has its base terminal VB applied with the proper DC bias potential and grounded in an AC manner.

Since the common emitter terminal of the differential amplifier that amplifies the first input signal is coupled via the common-base transistor 206 to the collector of the common-emitter transistor 207 that amplifies the second input signal, the gain of the differential amplifier is proportional to the collector current of the transistor 207. An output signal proportional to the product of the first and second input signals is therefore acquired from the output terminal OP, which means that the circuit shown in Fig. 13 will function as a multiplying circuit.

If the multiplying circuit is used as the frequency converter or demodulator of a receiver that receives and demodulates a minute signal, it is necessary to reduce the thermal noise generated by the base parasitic resistance of the common-emitter transistor 207 in order to make the noise factor as small as possible. In this respect, a transistor with a small base parasitic resistance or a relatively large emitter area is used for the common-emitter transistor 207. For the common-base transistor 206, a transistor with a small emitter area than that of the common-emitter transistor 207 is used. For instance, the emitter area ratio of the transistor 206 to the transistor 207 is determined to be 1:4.

Since the parasitic capacitance of the transistor 206 is smaller than that of the transistor 207, an impedance as viewed from the common emitter terminal of the differential amplifier toward the collector of the common-emitter transistor 207 is higher than the one in the conventional multiplying circuit which does not have the common-base transistor 206. It is therefore possible to suppress the CMRR from dropping due to the use of a transistor with a large emitter area for the common-emitter transistor 207, and reduce the leaking of the input signal from the input terminal pair LO1



and LO2 to the input terminal Rf.

Fig. 14 shows a multiplying circuit according to the seventh embodiment which includes three differential amplifiers for amplifying the first input signal and three common-base transistors. A first pair of differential transistors 301 and 304 constitute one of the differential amplifiers, a second pair of differential transistors 302 and 305 constitute another differential amplifier, and a third pair of differential transistors 303 and 306 constitute the last differential amplifier. These differential amplifiers have their output terminal pairs connected to a common load circuit 307 which is provided with an output terminal OP.

The common emitter terminals of the three differential amplifiers are connected to the collectors of the common-base transistors 308, 309 and 310, with the emitter of the transistor 308 connected to the collector of a common-emitter transistor 311. The common base terminal VB of the common-base transistors 308 to 310 is applied with the proper DC bias potential and grounded in an AC manner.

In this embodiment, the emitter area ratio of the transistors 301 and 306 to the transistors 302 to 305, all transistors constituting the differential amplifiers, is determined to be 4 : 1, and the emitter area of the transistor 308, to the transistor 309 and to the transistor 310 is set to 3 : 2 : 3, for example, a DC offset is given to the individual differential amplifiers, and a collector current proportional to the emitter area will flow through the common-base transistors. It is therefore possible to weight the distribution ratio of the currents flowing to the common emitter terminals of the individual differential amplifiers is weighted. This can provide linearity to the first input signal input to the input terminal pair LO1 and LO2. When this multiplying circuit is used as, for example, the frequency converter (mixer) of a receiver, with a local oscillator signal input to the input terminal pair LO1 and LO2 and a high frequency input signal input to the input terminal Rf, the harmonic of the local oscillator signal can be reduced. This will result in reduction of the amount of superimposition of the product of the interference wave or noise contained in the high frequency input signal and the local oscillator signal onto the desired output frequency.

Fig. 15 illustrates a multiplying circuit according to the eighth embodiment in which common-base transistors 312 to 314 (first common-base transistors) having a small emitter area are inserted between the common emitter terminals of the differential amplifiers in Fig. 14 and weighting common-base transistors 308 to 310 (second common-base transistors). The common base terminal VB1 of the transistors 308 to 310 and the common base terminal VB2 of the transistors 312 to 314 are applied with the proper DC bias potentials and are grounded in an AC manner.

This embodiment therefore has an effect of suppressing the dropping of the CMRR caused by tran-

sistors with a large emitter area and large parasitic capacitance, included in the weighting common-base transistors 308-310, by means of the additional common-base transistors 312 to 314, thus reducing the amount of the signal input to the input terminal pair LO1 and LO2 from leaking to the input terminal Rf, in addition to the advantage of the seventh embodiment in Fig. 14.

Fig. 16 shows a multiplying circuit according to the ninth embodiment, a preferable exemplary multiplying circuit to be used as an orthogonal demodulator in a receiver in a direct conversion system. The multiplying circuit comprises a combination of two of the multiplying circuits shown in Fig. 13 as a unit multiplying circuit. The two multiplying circuits share one common-emitter transistor.

In Fig. 16, the two unit multiplying circuits have pairs of input terminals LO1 and LO2, and LO3 and LO4, respectively. In the case of multiplying circuit as an orthogonal demodulator, an input signal at the input terminal pair LO1 and LO2 and that at the input terminal pair LO3 and LO4 are local oscillator signals whose phases are mutually shifted by 90°. A signal to be demodulated, i.e., a modulated signal is input to another input terminal Rf.

The input signal at the input terminal pair LO1 and LO2 is amplified by a differential amplifier having transistors 401 and 402, and is sent from a load resistor 405 to an output terminal OP11. The input signal at the input terminal pair LO3 and LO4 is amplified by a differential amplifier having transistors 403 and 404, and is sent from a load resistor 406 to an output terminal OP12. The second input signal at the input terminal Rf is amplified by a common-emitter transistor 409. This transistor 409 has a base connected to the input terminal Rf and an emitter grounded.

The common emitter terminal of the transistors 401 and 402 and that of the transistors 403 and 404 are respectively connected to the collectors of common-base transistors 407 and 408. The emitters of the common-base transistors 407 and 408 are commonly connected to the collector of the common-emitter transistor 409. A proper DC bias potential is applied to a common base terminal VB of the common-base transistors 407 and 408, which is grounded in an AC manner.

The two differential amplifiers, which amplify the respective the local oscillator signals with their phase shifted by 90° each other, have their common emitter terminals connected via the respective common-base transistors 407 and 408 to the collector of the common-emitter transistor 409 which amplifies a modulated signal. A demodulation output with a phase shifted by 90°, i.e., an orthogonal demodulation output is yielded from the output terminals OP11 and OP12.

In this embodiment, the common-base transistors 407 and 408 reduce an influence on the parasitic



capacitance of the common-emitter transistor 409 whose emitter area is enlarged to decrease a parasitic resistance, and distribute the output current (collector current) of the common-emitter transistor 409 to the two differential amplifiers.

An orthogonal demodulator is required to reduce a phase difference and a conversion gain difference. In a conventional orthogonal demodulator, a modulated signal to be demodulated is divided into two signals, which are in turn sent to two independent multiplying circuits where local oscillation signals with their phases shifted by 90° each other is supplied. In an orthogonal demodulator employing the multiplying circuit in Fig. 16, a modulated signal is input to the base of a common-emitter transistor shared by two multiplying circuits, which perform distribution on the signal and multiplication (orthogonal demodulation) on the distributed signals to a local oscillator signal. The orthogonal demodulator using the multiplying circuit in Fig. 16 therefore have fewer components through which a modulated signal passes than those of the conventional one. This can decrease factors causing a difference and reduce a phase difference and a conversion gain difference.

In the embodiment in Fig. 16, the multiplying circuit shown in Fig. 13 has been used as two basic unit multiplying circuits, but any of the multiplying circuit shown in Figs. 14 to 17 may be used instead. Further, three or more unit multiplying circuits can be combined, sharing a common-emitter transistor.

The present invention can therefore provide a multiplying circuit which has less decrease in the CMRR at a high frequency and in signal leak from input terminals where two signals to be multiplied are input, and a broad linearity range with slight deformation.

Accordingly, using the multiplying circuit in a transmitter, for example, it is possible to acquire a transmission output having a low carrier leak and small deformation. The multiplying circuit when used in a receiver can make noise low, widen a dynamic range, and reduce the amount of undesired radiation due to the leakage of a local oscillator signal to an antenna system.

## Claims

1. A multiplying circuit characterized by comprising:
  - first and second differential amplifiers (1,2; 3,4) for receiving a first input signal, and each having an output terminal pair and a common emitter terminal;
  - output means (OP1, OP2), connected to said output terminal pairs of said first and second differential amplifiers connected in such a way as to cancel out outputs thereof each other, for providing a difference between said outputs of said

first and second differential amplifiers as an output signal;

first and second common-base transistors (13, 14) having bases tied to a constant potential and collectors connected to said common emitter terminals of said first and second differential amplifiers; and

multiple third differential amplifiers (5-7) for receiving a second input signal and each having an output terminal pair connected commonly to said emitters of said first and second common-base transistors and having predetermined DC offsets.

2. A multiplying circuit according to claim 1, characterized in that each of said third differential amplifiers comprises a pair of transistors (5,7; 6,8) designed to have a predetermined emitter area ratio to acquire a predetermined DC offset.

3. A multiplying circuit according to claim 1, characterized in that said first and second common-base transistors (1,2; 3,4) each have an emitter area smaller than a maximum emitter area of transistors used in each of said third differential amplifiers.

4. A multiplying circuit according to claim 1, characterized in that said third differential amplifiers are constituted by two pairs of transistors (5,7; 6,8), one having an emitter area ratio of 4 : 1, and the other 1 : 4.

5. A multiplying circuit according to claim 1, characterized in that said third differential amplifiers are constituted by three pairs of transistors (49,52; 50,53; 51,54), a first one having an emitter area ratio of 8 : 1, a second one 1 : 1, and a third one 1 : 8.

6. A multiplying circuit according to claim 1, characterized in that said third differential amplifiers are constituted by four pairs of transistors (21,25; 22,26; 23,27; 24,28), a first one having an emitter area ratio of 13 : 1, a second one 2 : 1, a third one 1 : 2, and a forth one 1 : 13.

7. A multiplying circuit characterized by comprising:
 

- multiple first differential amplifiers (41-43) and multiple second differential amplifiers (45-48) for receiving a first input signal, each of said first and second differential amplifiers having an output terminal pair, a common emitter terminal and a predetermined DC offset;

output means (OP1, OP2), connected to said output terminal pairs of said first and second differential amplifiers connected in such a way as to cancel out outputs of said first and second dif-

ferential amplifiers each other, for providing a difference between said outputs of said first and second differential amplifiers as an output signal;

multiple first common-base transistors (58, 59) having bases tied to a constant potential, collectors connected to said common emitter terminals of said multiple first differential amplifiers and emitters commonly connected;

multiple second common-base transistors (60, 61) having bases tied to a constant potential, collectors connected to said common emitter terminals of said multiple second differential amplifiers and emitters commonly connected; and

multiple third differential amplifiers (49-54) for receiving a second input signal and each having a pair of output terminals connected to said common emitter terminals of said first and second common-base transistors so as to have predetermined DC offsets.

8. A multiplying circuit according to claim 7, characterized in that each of said third differential amplifiers comprises a pair of transistors (49,52; 50,53; 51,54) designed to have an emitter area ratio in order to acquire a predetermined DC offset, and each of said first and second common-base transistors has a smaller emitter area than a maximum emitter area of said pair of transistors constituting each of said third differential amplifiers.

9. A multiplying circuit characterized by comprising: multiple first differential amplifiers (41-44) and multiple second differential amplifiers (45-48) for receiving a first input signal and each having an output terminal pair, a common emitter terminal and a predetermined DC offset;

output means (OP1, OP2), connected to said output terminal pairs of said first and second differential amplifiers connected in such a way as to cancel out outputs of said first and second differential amplifiers each other, for providing a difference between said outputs of said first and second differential amplifiers as an output signal;

multiple first common-base transistors (58, 59) having bases tied to a constant potential, collectors connected to said common emitter terminals of said multiple first differential amplifiers and emitters commonly connected having a predetermined emitter area ratio;

multiple second common-base transistors (60, 61) having bases tied to a constant potential different from the constant potential applied to said first common-base transistors, collectors connected to said common emitter terminals of said multiple second differential amplifiers and emitters commonly connected and having said

predetermined emitter area ratio; and

multiple third differential amplifiers (49-54) for receiving a second input signal and each having a pair of output terminals connected to said common emitter terminals of said first and second common-base transistors and having predetermined DC offsets.

10. A multiplying circuit according to claim 9, characterized in that each of said first, second and third differential amplifiers comprises at least one pair of transistors designed to have a predetermined emitter area ratio to acquire a predetermined DC offset

11. A multiplying circuit characterized by comprising: multiple first differential amplifiers (71-76) and multiple second differential amplifiers (77-82) for receiving a first input signal, each of said first and second differential amplifiers having an output terminal pair, a common emitter terminal and a predetermined DC offset;

output means (OP1, OP2), connected to said output terminal pairs of said first and second differential amplifiers connected in such a way as to cancel out outputs of said first and second emitter coupled transistor pairs each other, for providing a difference between said outputs of said first and second differential amplifiers as an output signal;

multiple first common-base transistors (105-107) having bases tied to a constant potential, collectors connected to said common emitter terminals of said multiple first differential amplifiers;

multiple second common-base transistors (108-110) having bases tied to a constant potential, collectors connected to said common emitter terminals of said multiple second differential amplifiers;

multiple third common-base transistors (91-93) having bases tied to a constant potential different from the constant potential applied to said first common-base transistors; collectors connected to said emitters of said multiple first common-base transistors and emitters commonly connected so as to have a predetermined emitter area ratio;

multiple fourth common-base transistors (94-96) having bases tied to a constant potential different from the constant potential applied to said second common-base transistors, collectors connected to said emitters of said multiple second common-base transistors and emitters commonly connected so as to have the predetermined emitter area ratio; and

multiple third differential amplifiers (101-104) for receiving a second input signal and each

having a pair of output terminals connected to said common emitter terminals of said first and second common-base transistors and having predetermined DC offsets.

12. A multiplying circuit according to claim 11, characterized in that each of said first, second and third differential amplifiers (71-76; 77-82; 101-104) comprises a pair of transistors designed to have a predetermined emitter area ratio to acquire a predetermined DC offset.

13. a multiplying circuit according to claim 11, wherein said first and second common-base transistors (105-107; 108-110) each have an emitter area smaller than a maximum emitter area of said third and fourth common-base transistors (91-93; 94-96).

14. A multiplying circuit characterized by comprising: a differential amplifier (201; 202) for receiving a first input signal and having an output terminal pair and a common emitter terminal;

a load circuit (204; 205) connected to at least one output terminal of said output terminal pair of said differential amplifier;

a common-emitter transistor (207) having a base supplied with a second input signal; and a common-base transistor (206) having a base tied to a constant potential, a collector connected to said common emitter terminal of said differential amplifier, and an emitter connected to a collector of said common-emitter transistor and having a smaller emitter area than said common-emitter transistor.

15. A multiplying circuit characterized by comprising: multiple differential amplifiers (301-306) for receiving a first input signal and each having an output terminal pair, a common emitter terminal and a predetermined DC offset;

a load circuit (307) connected to at least one output terminal of each of said output terminal pairs of said differential amplifiers;

a common-emitter transistor (311) having a base supplied with a second input signal; and multiple common-base transistors (308-310) having bases tied to a constant potential, collectors connected to said common emitter terminals of said multiple differential amplifiers, and emitters connected to a collector of said common-emitter transistor and having a predetermined emitter area ratio.

16. A multiplying circuit comprising: multiple differential amplifiers (301-306) for receiving a first input signal and each having an output terminal pair, a common emitter terminal

and a predetermined DC offset;

a load circuit (307) connected to at least one output terminal of each of said output terminal pairs of said differential amplifiers;

a common-emitter transistor (311) having a base supplied with a second input signal; and multiple first common-base transistors (308-310) having bases tied to a constant potential, and emitters connected to a collector of said common-emitter transistor and having a predetermined emitter area ratio; and

multiple second common-base transistors (312-314) having bases tied to a constant potential, collectors respectively connected to said common emitter terminals of said multiple differential amplifiers, and emitters respectively connected to collectors of said multiple first common-emitter transistors and having emitter areas equal to or smaller than a minimum emitter area of one of said multiple first common-base transistors.

17. A multiplying circuit apparatus characterized by comprising:

a plurality of multiplying circuits; and

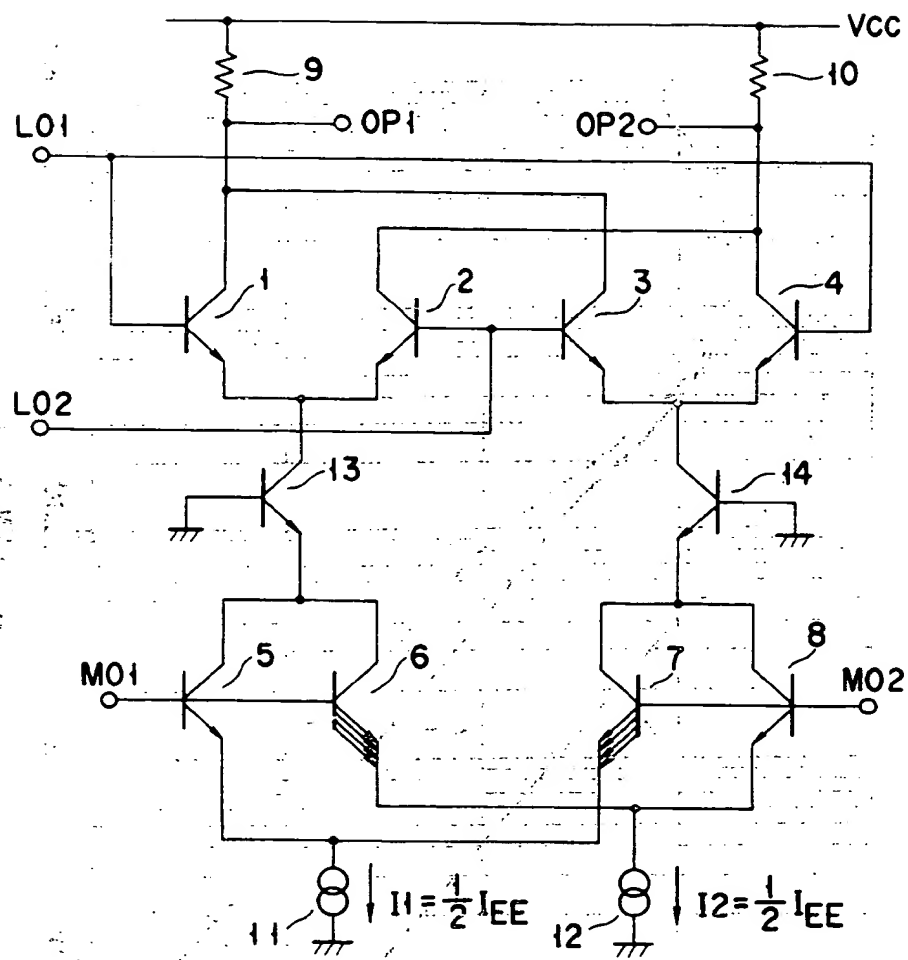
a common-emitter transistor commonly connected to said plurality of multiplying circuits, each of said plurality of multiplying circuits comprising,

first and second differential amplifiers (1,2; 3,4) for receiving a first input signal and each having an output terminal pair and a common emitter terminal;

output means (OP1, OP2), connected to said output terminal pairs of said first and second differential amplifiers connected in such a way as to cancel out outputs thereof each other, for providing a difference between said outputs of said first and second differential amplifiers as an output signal;

first and second common-base transistors (13, 14) having bases tied to a constant potential and collectors connected to said common emitter terminals of said first and second differential amplifiers; and

multiple third differential amplifiers (5,6; 6,7) for receiving a second input signal and each having an output terminal pair connected commonly to said emitters of said first and second common-base transistors and having predetermined DC offsets.



F I G. 1

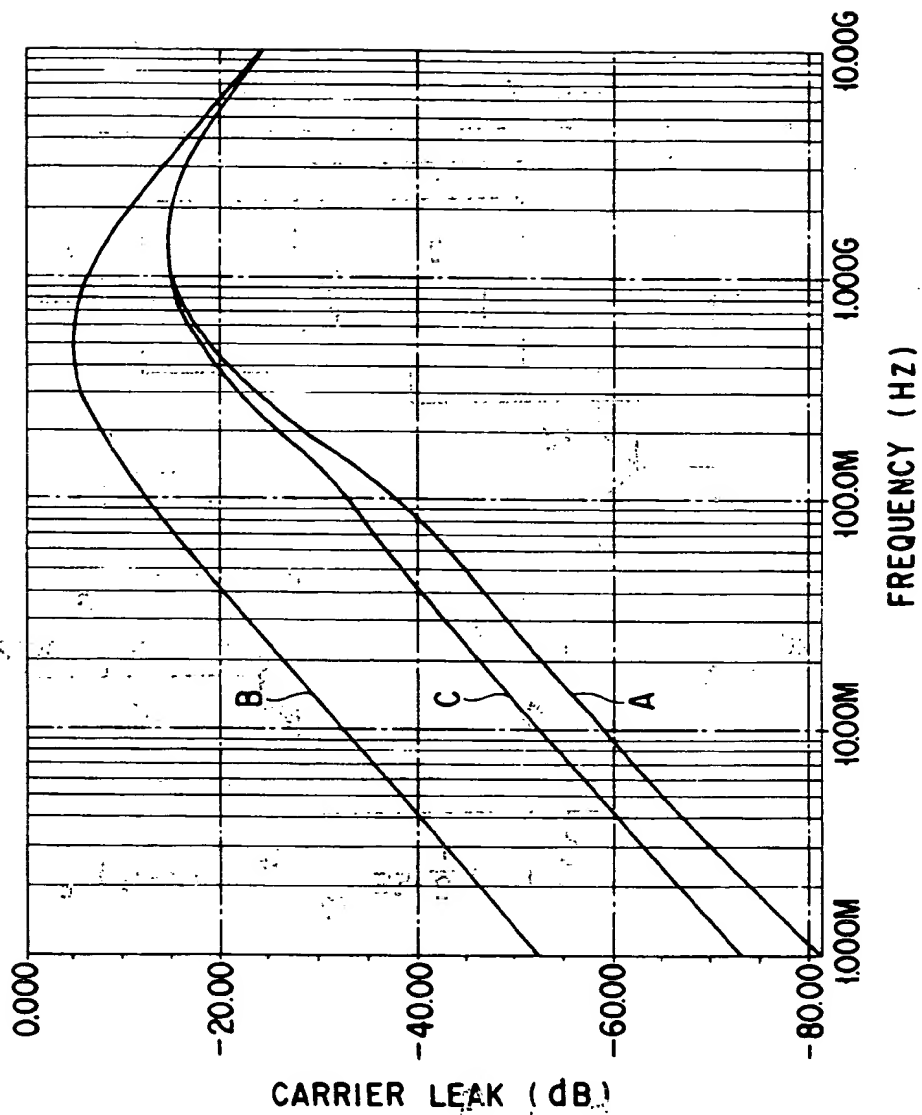


FIG. 2

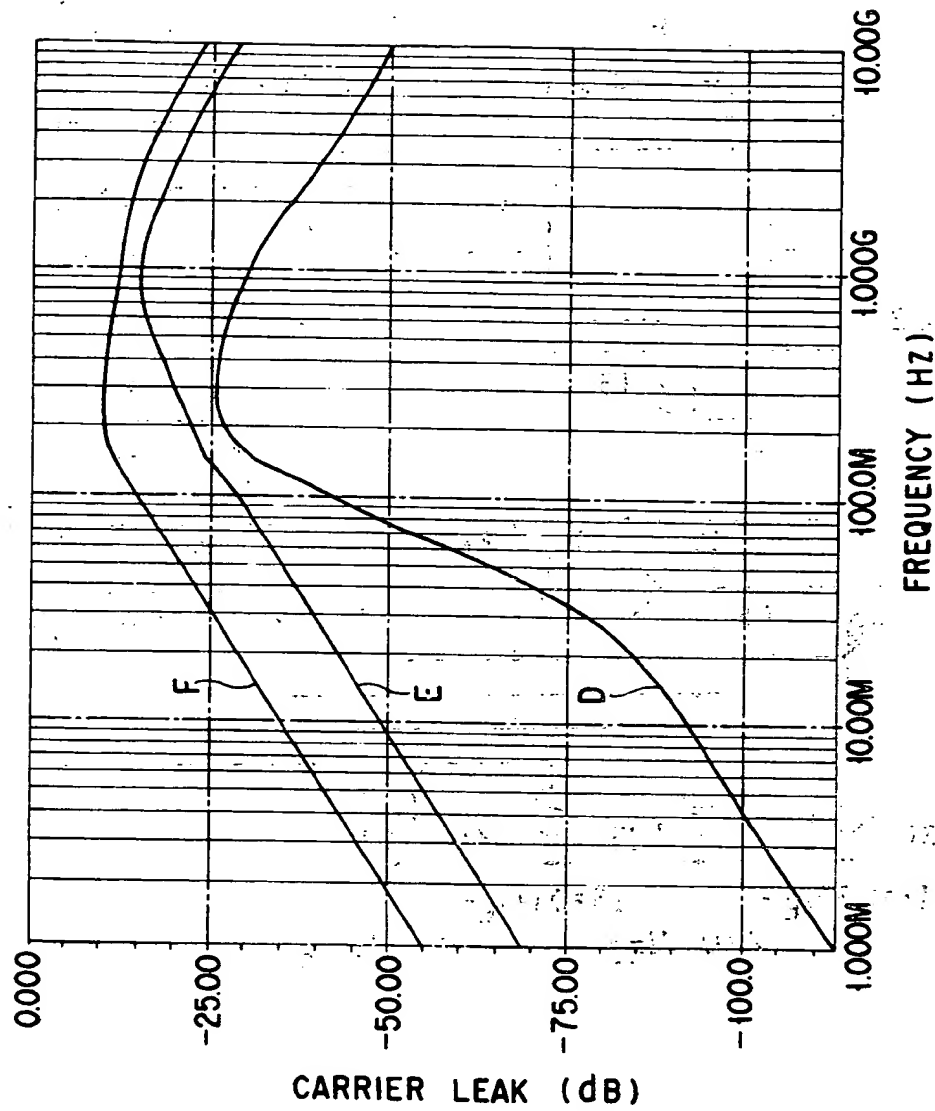


FIG. 3

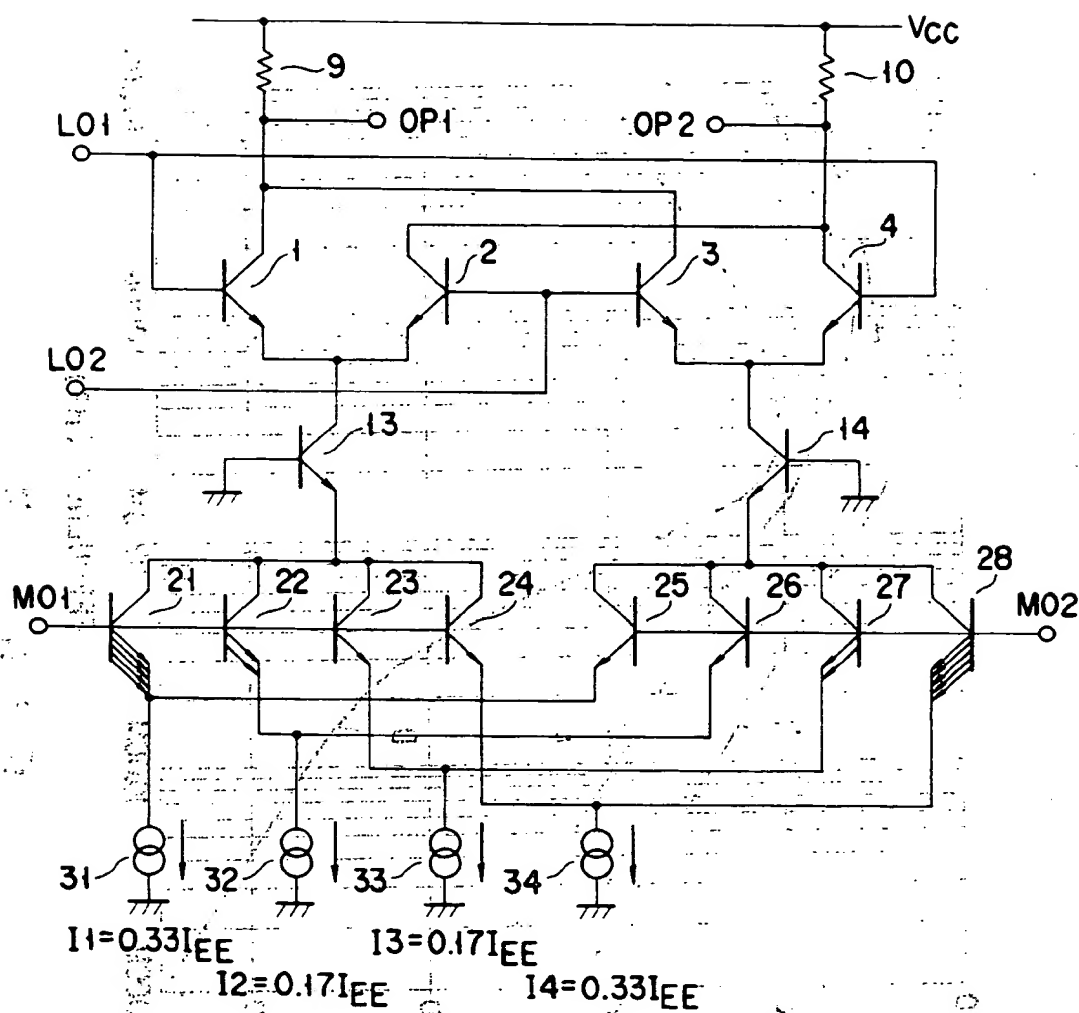


FIG. 4



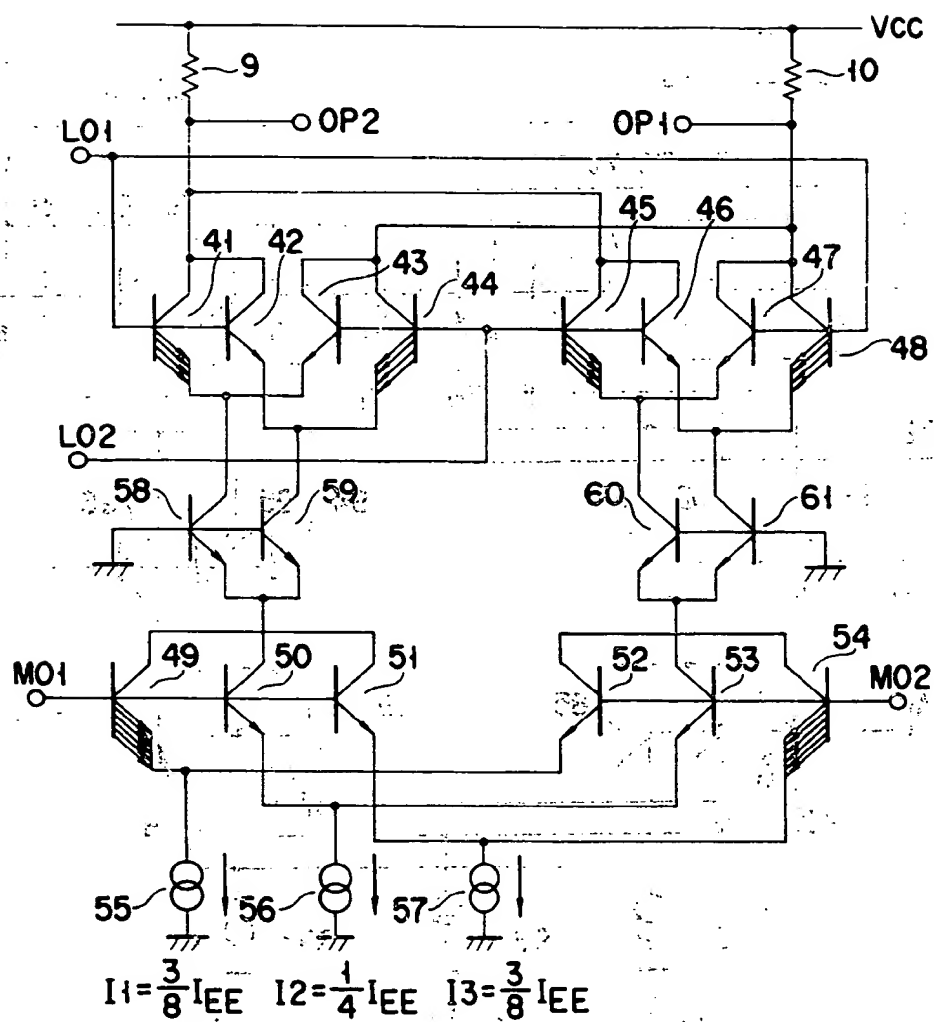


FIG. 5

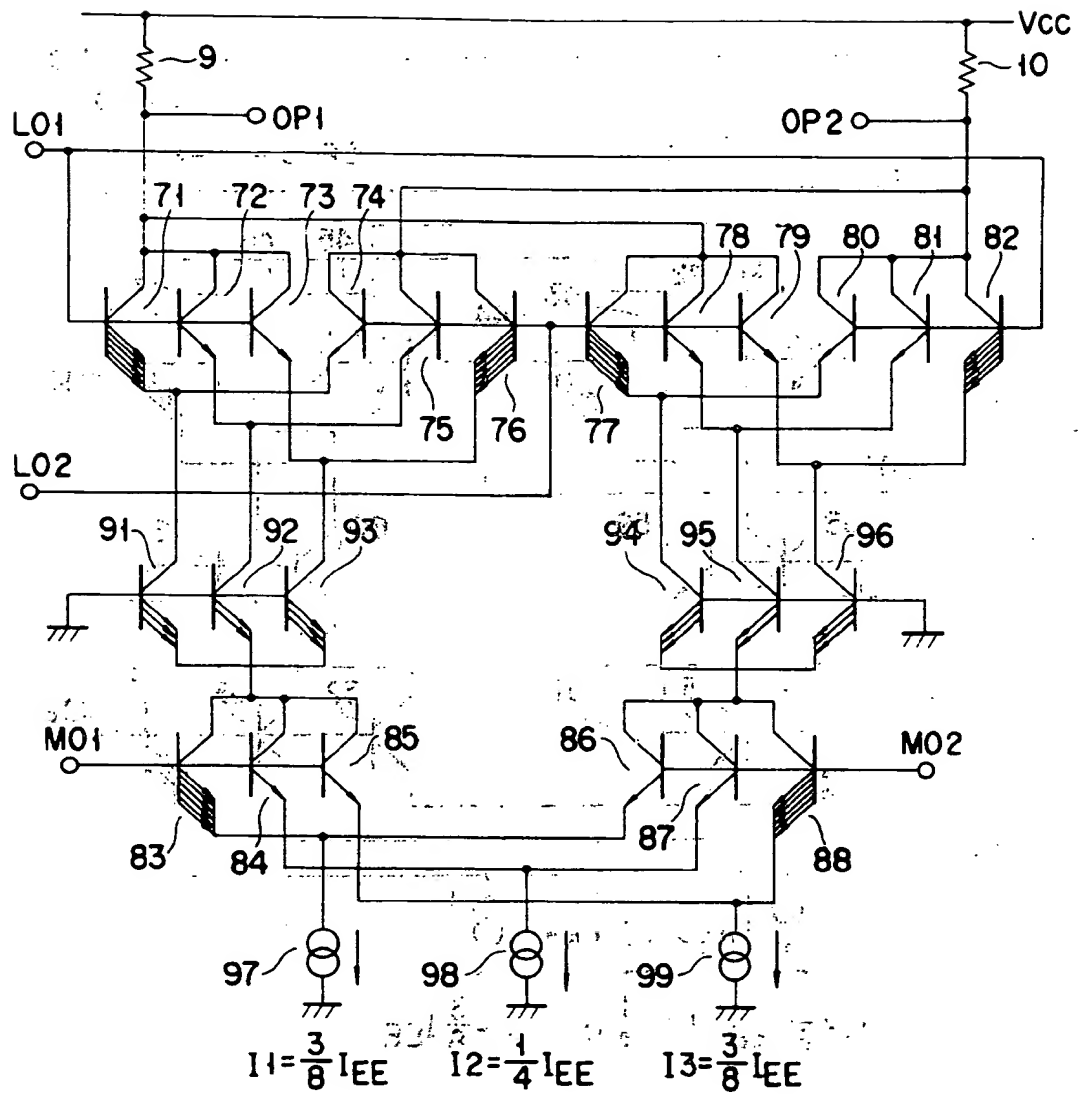


FIG. 6

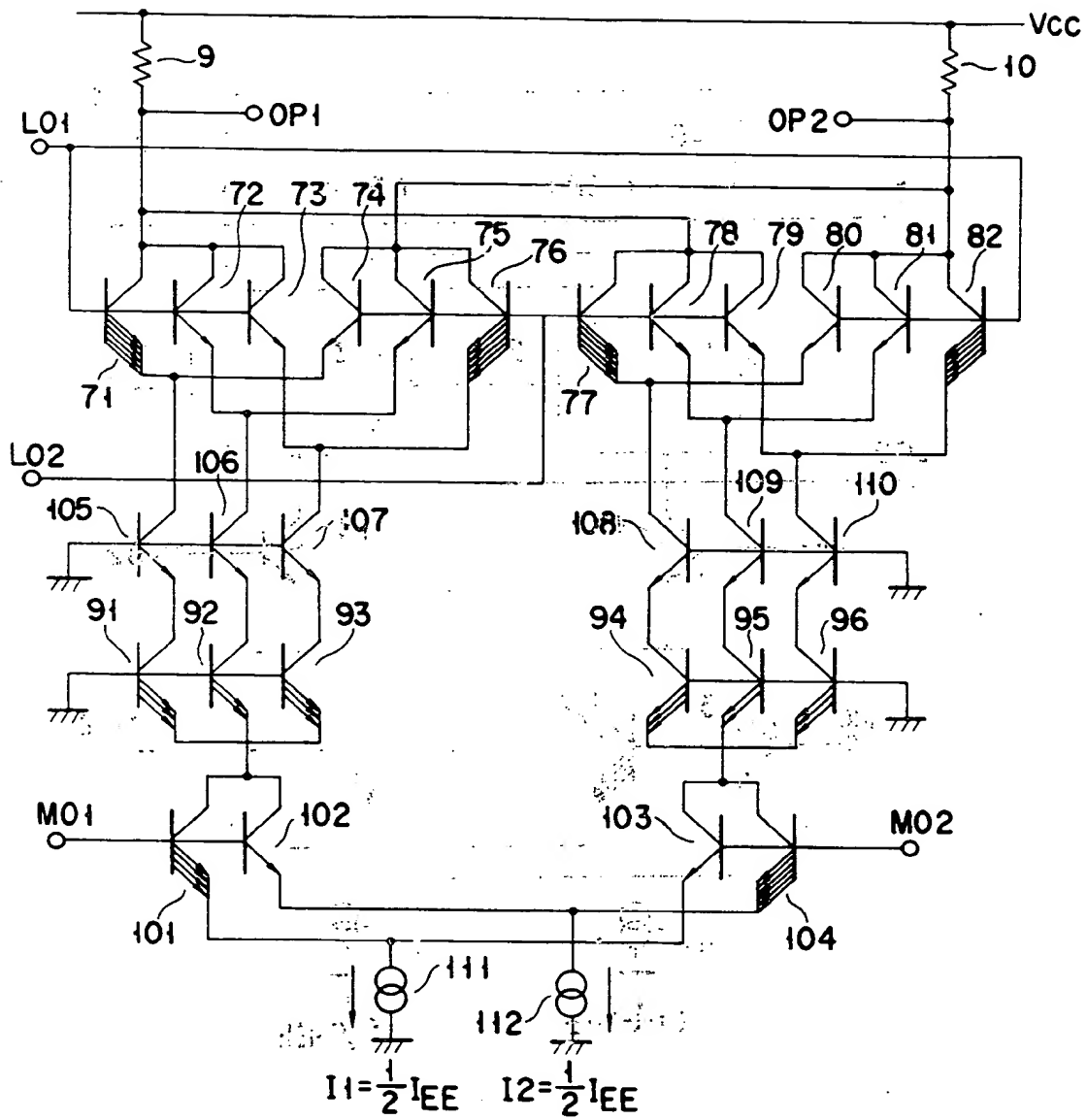
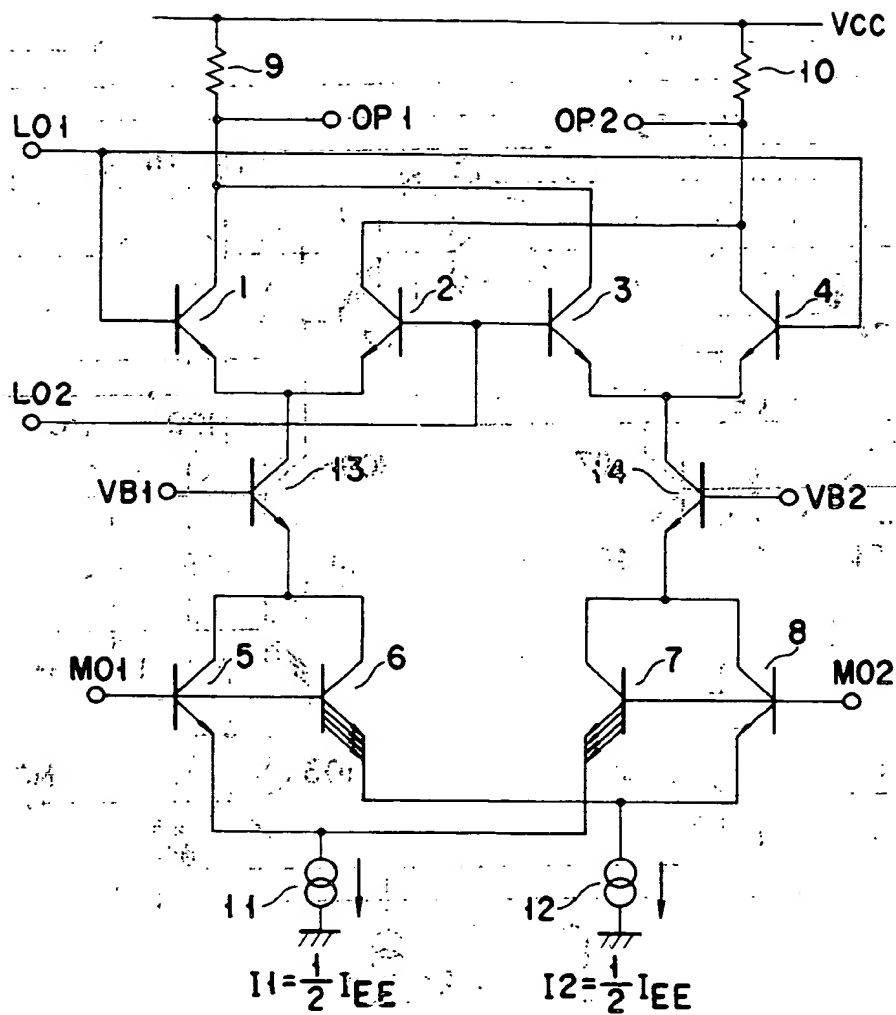
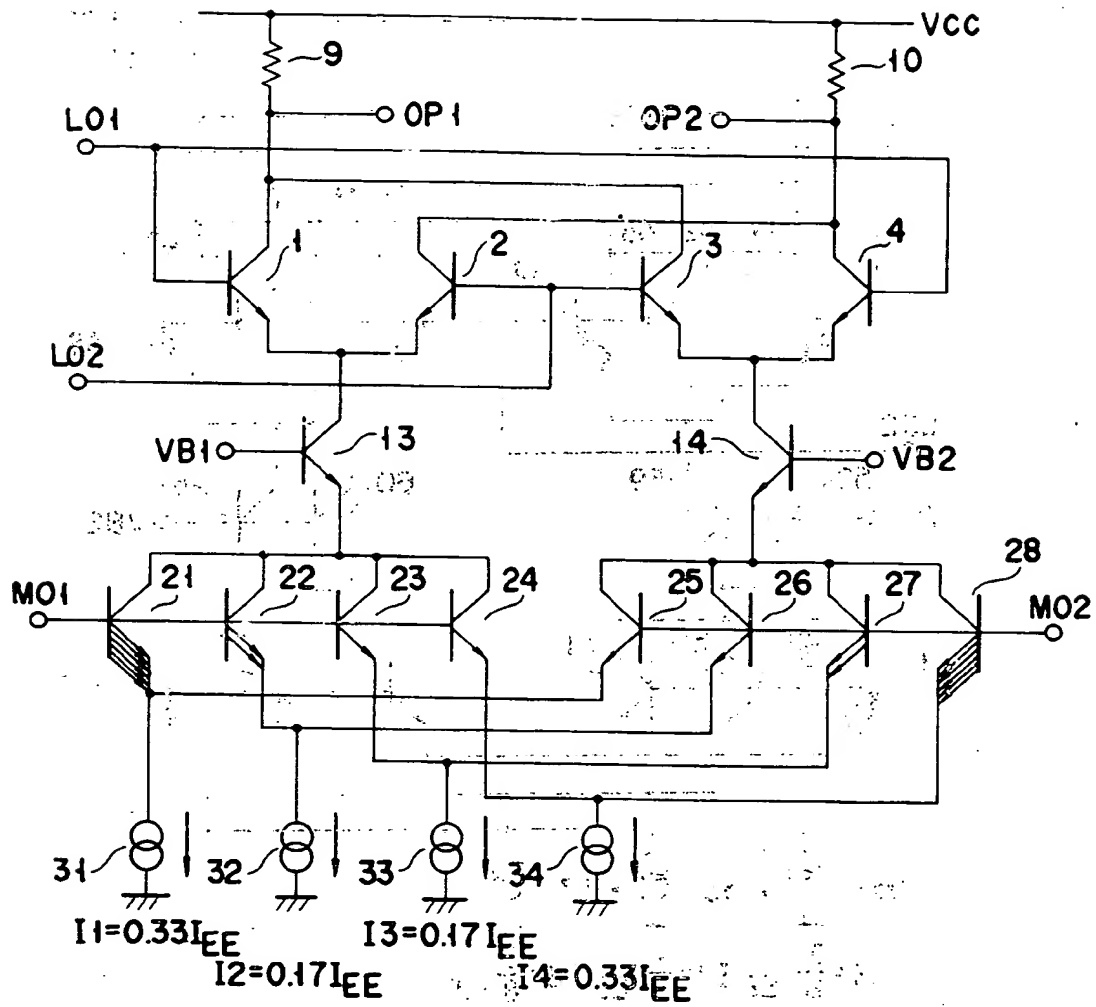


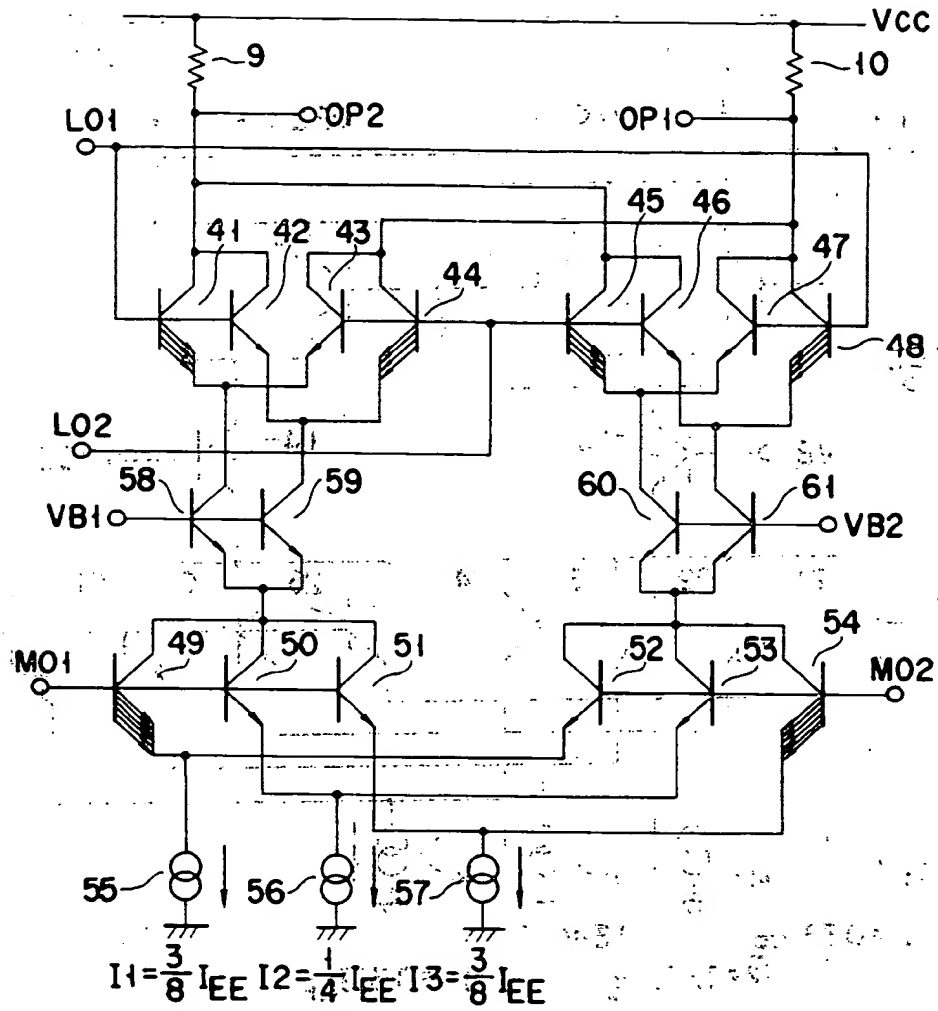
FIG. 7



F I G. 8



F I G. 9



F I G. 10





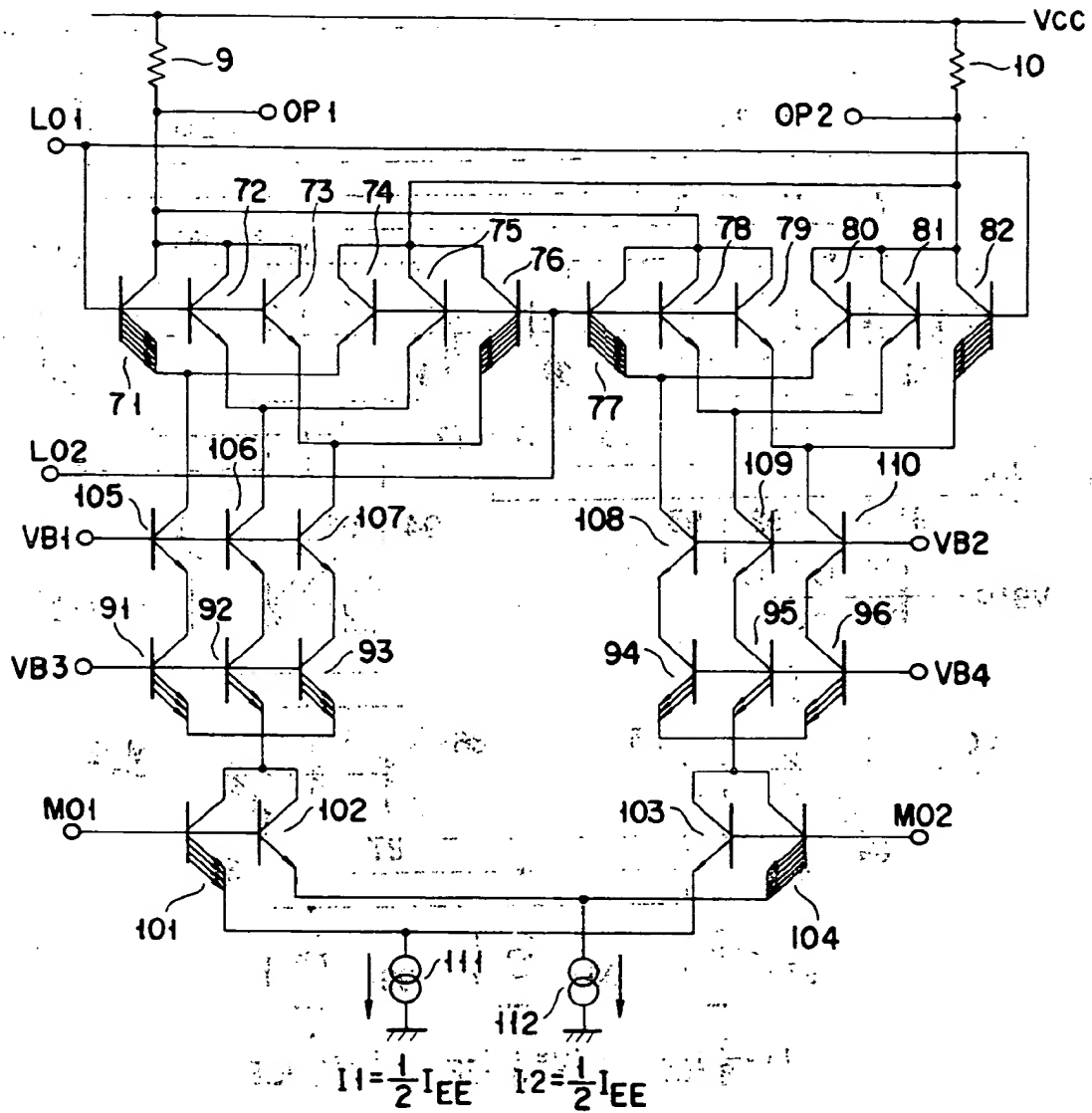
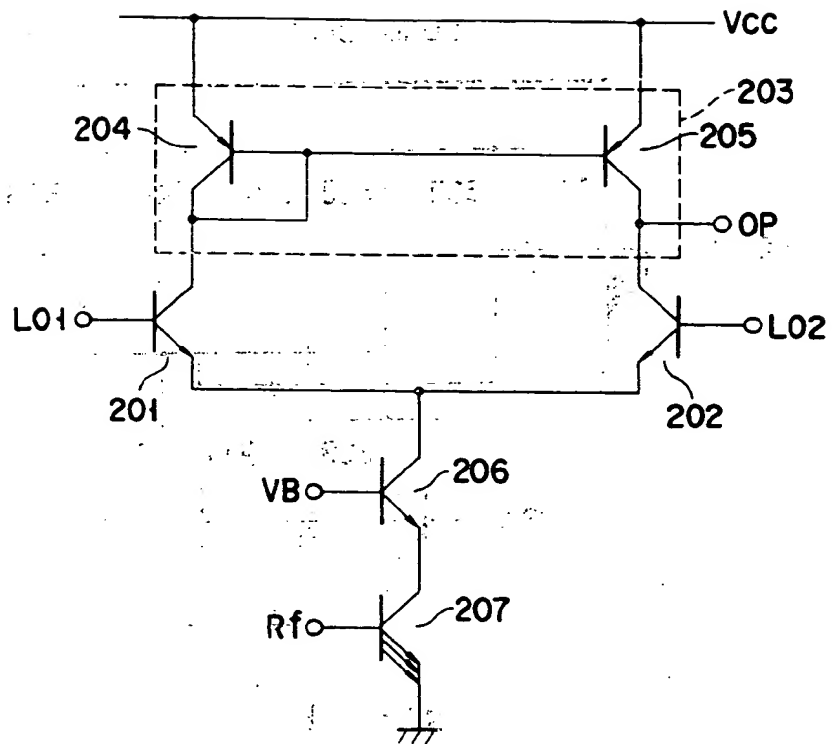
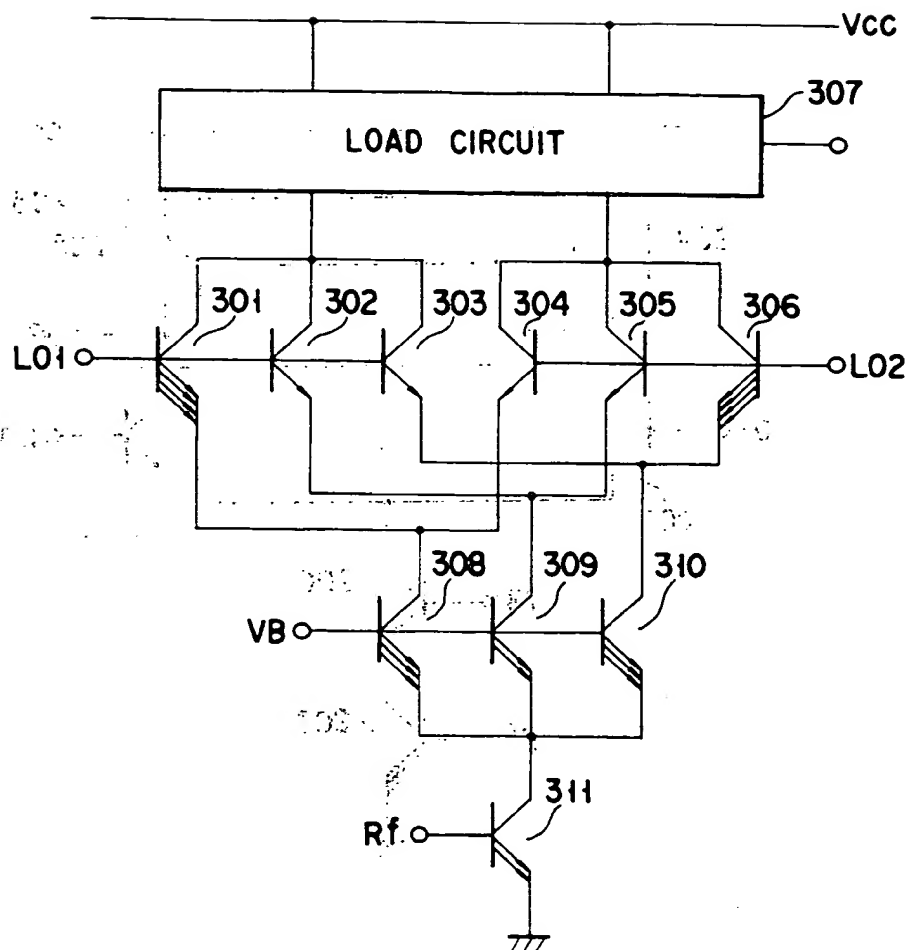


FIG. 12

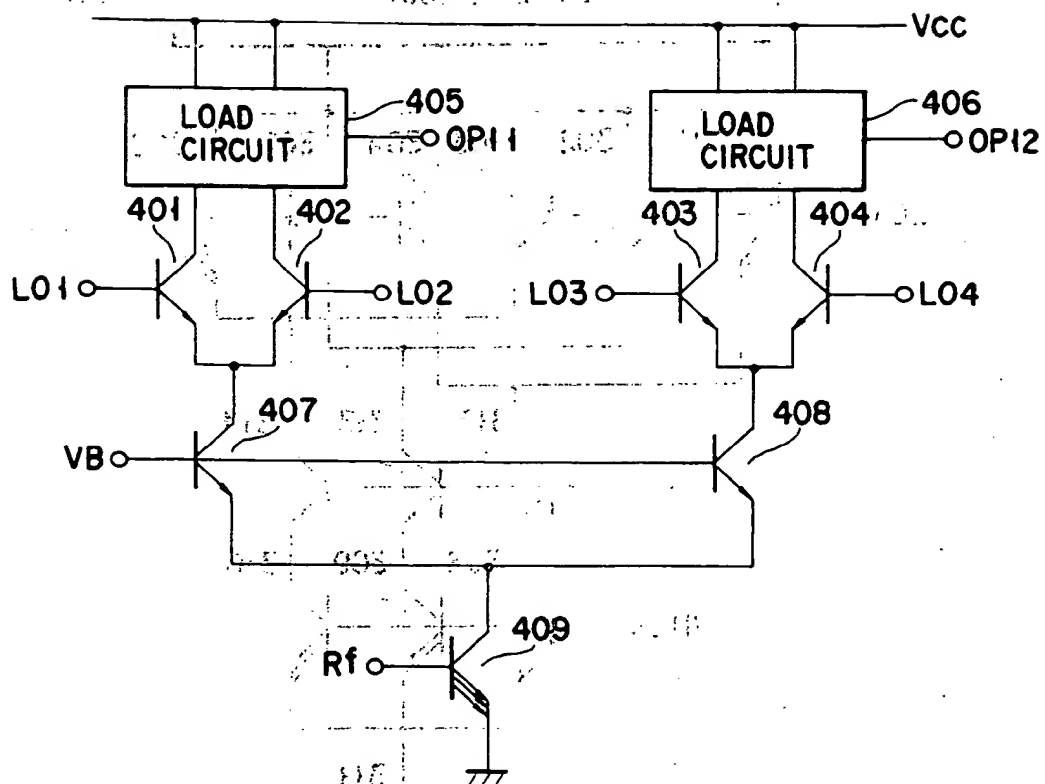


F I G. 13



F I G. 14





F I G. 16

